CAREER OBJECTIVE

As a passionate Electrical Engineering undergraduate student, I aim to contribute my technical knowledge and innovative problem-solving abilities to some exciting projects, where I can further develop my expertise in these fields and have a meaningful impact to the society.

EDUCATION

Degree/Certificate	**Institute/Board**	**CGPA / Percentage**	**Year**
B.Tech (Electrical Engineering)	IIT, Palakkad	9.04 (Current)	2022-Present
Class XII	Central Academy, Dadabari, Kota, Rajasthan	89%	2021
Class X	SBD International School, Samaraipur, Bhadrak, Odisha	96%	2019

TECHNICAL SKILLS

- **Verilog**
- **Python**
- **Cadence Modus**
- **Xcelium**
- **Vmanager**
- **LTspice**
- **Matlab**

WORK EXPERIENCE

- **Digital Design Intern** **May 2025 to Jul 2025**
  Texas Instruments
  Exploration of LPG(Low Power Gating) in DFT using Cadence Modus. VManager Automation for Failed Vectors Dump in DFT Simulations. Exploration of Verisiums apps like Codeminer,Waveminer and Verisium Debug.
- **Hardware engineering Intern** **Jan 2026 to Jul 2026**
  Morphing Machines
  Algorithm to architecture mapping.

PROJECTS

- **Information Lattice Learning (ILL)** **Aug 2025 to Dec 2025**
  Dr. Subrahmanyam Mula and Dr. Vinay Chakravarthi Gogineni
  UG project
  Engineered a high-performance architecture for the Information Lattice Learning (ILL) model, enabling "one-shot" image recognition with 84% accuracy on MNIST (vs. 16% for ViT based models). Optimized the core spatial smoothing bottleneck by formulating a FFT-based frequency domain approach, reducing computational complexity from qudratic to logarithmic dependency and cutting FLOPs by over 99% while maintaining geometric robustness and accuracy. *Link*

- **Hyperspectral Anomaly Detection** **Jan 2025 to May 2025**
  Dr. Subrahmanyam Mula and Dr. Vinay Chakravarthi Gogineni
  OELP
  Engineered a Fused Autoencoder (CNN-ViT) for unsupervised hyperspectral anomaly detection, achieving state-of-the-art performance with an AUC of 0.99 on benchmark datasets. Optimized the model by implementing an efficient FFT-based ViT, reducing inference time by over 55% and lowering FLOPs while maintaining high accuracy. *Link*

- **Systolic Array based 1D/2D DCT Processor Implementation** **Apr 2025 to May 2025**
  Dr. Subrahmanyam Mula
  Course project
  Designed and implemented a pipelined, systolic array architecture for an 8-point 1D Discrete Cosine Transform (DCT) processor in Verilog HDL. Extended the modular 1D core to build a 2D DCT processor. *Link*

- **EEG Based Emotion Recognition for Stress Analysis (Spectrogram, 2DCNN)** **Mar 2024 to May 2024**
  Dr. M. Sabarimalai Manikandan
  Course project
  This project developed a model to predict stress levels from EEG data using 2D Convolutional Neural Network model. Spectrograms generated from the EEG signals were processed by a 2D Convolutional Neural Network (2DCNN) to classify the stress levels. Achieving an overall accuracy of 96%, the study demonstrated the efficacy of CNNs in real-time emotion recognition by automating feature extraction. *Link*

- **Building a 8 bit microprocessor in Logisim with minimal functions** **Mar 2024 to Apr 2024**
  Dr. Vijay Murlidharan
  Course project
  Building a 8 bit microprocessor using Logisim Evolution with 8 bit address and data buses, including registers (R0, R1, R2) and adder and AND operators. Instructions like JUMP, MOV, ADD, AND, and COPY are to be implemented.

ELECTIVE COURSES

- VLSI Design
- VLSI Architectures for Signal Processing and Machine Learning
- Reinforcement Learning
- Robot Implementation Methods
- Computer Graphics
- PCB Design

EXTRA CURRICULAR ACTIVITIES

- **General Championship - Table Tennis**
  I played Men's Doubles Table Tennis in the General Championship representing Batch 22.

- **NSO**
  Took part in NSO cricket